REMARKS

Claims 1-30 are currently pending. Claims 1, 12, and 29 have been amended. No new matter has been added. The support for the amendment can be found at least in paragraph 33 of the originally filed specification.

Interview Summary

The Examiner is gratefully thanked for conducting telephonic interviews with the undersigned attorney on September 7, 2007. Examiner's interpretation of claim 1 was discussed at the interview, and prior art Sheeran et al. was discussed. Specifically, it was agreed that Sheeran checks every state, which is different than the present claimed invention. It was agreed that Applicant will amend the claims to clarify that aspect. It was also agreed that Examiner will contact the Applicant, if necessary, after reviewing the amendment in order to place the claims in condition for allowance.

Claim Rejections Under 35 U.S.C. §102

Claims 1-30 were rejected under 35 U.S.C. §102(a) as anticipated by Sheeran (*Checking safety properties using induction and a SAT-solver*, November 2000, In Proc. Conference on Formal Methods in Computer-Aided Design). Applicant respectfully traverses.

As explained in the originally filed specification, the present claimed invention is able to combine the benefits of limiting the number of transitions checked and yet gain some assurance on the thoroughness of property checking beyond just bounded verification.

Applicant respectfully submits that the cited Sheeran reference does not disclose each and every limitation of independent claim 1.

Independent claim 1 recites the following limitations (emphasis added):

(a) performing bounded verification on a circuit design for a number of transitions, the bounded verification corresponding to a ***predetermined limit*** for a number of transitions, <u>wherein the predetermined limit is less than a total number of all reachable states</u>;

(b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process comprising the acts of:

including, in an inductive set of one or more states, a plurality of states of the circuit design, wherein the inductive set of one or more states includes at least states passing the first property of the circuit design;

transitioning by at least one step, in a forward direction, states of the inductive set passing at least the first property of the circuit design, resulting in transitioned states;

determining if the transitioned states of the inductive set pass at least the first property of the circuit design;

repeating at least the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set passing or failing at least the first property of the circuit design; and

(c) if the at least one property is not verified, then *increasing the limit* for the bounded verification and repeating from (a).

Claim 1 as amended explicitly recite that the predetermined limit is less than the total number of all reachable states. This feature is not taught or suggested by Sheeran. The Action asserts that, in Sheeran, the domain of transition T is the entire set of states S. Hence, Sheeran's domain is the entire set of states. On the other hand, the present claim 1 requires the limit for a number of transition to be less than the entire set of states. Thus, Sheeran does not anticipate the amended claim 1.

For at least the same reasons, it is respectfully submitted that independent claims 12 and 29, including claims dependent thereon, are also allowable over the cited reference.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.
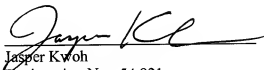
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Respectfully submitted,

Dated: September 10, 2007

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